## REMARKS

Claims 1 and 3-20 remain pending with claims 1, 7, and 15 being independent.

The remainder of the remarks follow a copy of the Office Action text in small, bolded letters:

**Claims 1 and 3-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirk (USP 4,709,347) in view of Mohamed (USP 6,366,998).**

**With respect to claim 1, 7, 15, Kirk teaches a method of processing network data (see Local Area Network 10 in Figure 1 of Kirk and lines 2-11 of column 4), in a processor (MOD) having multiple programmable multi-threaded (bit-slice) engines (see programmable micro-engine 18-04 in BIU of Figure 2 and lines 23-39 of column 4) integrated within the processor, the method comprising:**

**scheduling a first thread provided by multiple programmable multi-threaded engines (see programmable micro-engines) integrated within the processor to process a first incoming block of data within a network packet (packet is inherent in network system) received at a port (see transceiver 18-04 of Fig. 2) of a media access control device.**

**It appears that Kirk has only one (micro) engine instead of plurality...**

Claim 1 recites "multiple programmable multi-threaded engines". The Examiner argues that the microengine in the "BIU" of Kirk is multi-threaded, apparently equating each bit-slice component of the Kirk microengine with program threads. Applicants disagree that a bit-slice of the Kirk microengine is a thread.

As described in Kirk the "microengine 18-04 is made up of bit slice components so that it can process eight bits in parallel..." (col. 4, lines 24-27). More explicitly stated in the application (Ser. No. 06/540,062, "Method for Passing a Token in a Local-Area Network, U.S.P. 4,556,974) incorporated by reference into Kirk on col. 4, lines 42-47 of Kirk "microengine 22-05 is an 8-bit-wide arithmetic and logic unit made of bit slice components" (col. 5, lines 2-4 of the '974 patent). As made clear by these statements, the BIU microengine ALU (Arithmetic Logic Unit) of Kirk is constructed using a conventional bit-slice ALU hardware architecture well known in the art (e.g., an 8-bit ALU is constructed by combining the hardware of 8 1-bit ALUs in parallel). Of course, a 1-bit ALU is not the same thing as a software thread.

Thus, Applicant asks the Examiner to withdraw the rejections of the claims 1, 7, and 15 and their respective dependent claims for at least the reasons above.

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